connecting the leads of the device together until the device is to be inserted in the system. The shorting ring prevents the possibility of applying a potential across any two terminals of the device. With the ring the potential difference between any two terminals is maintained at 0 V. At the very least always touch ground to permit discharge of the accumulated static charge before handling the device, and always pick up the transistor by the casing.

There are often transients (sharp changes in voltage or current) in a network when elements are removed or inserted if the power is on. The transient levels can often be more than the device can handle, and therefore the power should always be off when network changes are made.

The maximum gate-to-source voltage is normally provided in the list of maximum ratings of the device. One method of ensuring that this voltage is not exceeded (perhaps by transient effects) for either polarity is to introduce two Zener diodes, as shown in Fig. 5.41. The Zeners are back to back to ensure protection for either polarity. If both are 30-V Zeners and a positive transient of 40 V appears, the lower Zener will "fire" at 30 V and the upper will turn on with a 0-V drop (ideally—for the positive "on" region of a semiconductor diode) across the other diode. The result is a maximum of 30 V for the gate-to-source voltage. One disadvantage introduced by the Zener protection is that the off resistance of a Zener diode is less than the input impedance established by the SiO_2 layer. The result is a reduction in input resistance, but even so it is still high enough for most applications. So many of the discrete devices now have the Zener protection that some of the concerns listed above are not as troublesome. However, it is still best to be somewhat cautious when handling discrete MOSFET devices.

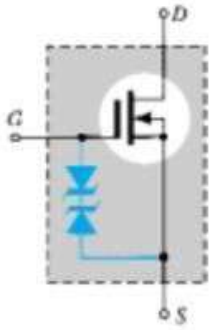

Figure 5.41 Zener-protected MOSFET.

5.10 VMOS

One of the disadvantages of the typical MOSFET is the reduced power-handling levels (typically, less than 1 W) compared to BJT transistors. This shortfall for a device with so many positive characteristics can be softened by changing the construction mode from one of a planar nature such as shown in Fig. 5.23 to one with a vertical structure as shown in Fig. 5.42. All the elements of the planar MOSFET are present in the vertical metal-oxide-silicon FET (VMOS)—the metallic surface connection to the terminals of the device—the SiO_2 layer between the gate and the *p*-type region between the drain and source for the growth of the induced *n*-channel (enhancement-

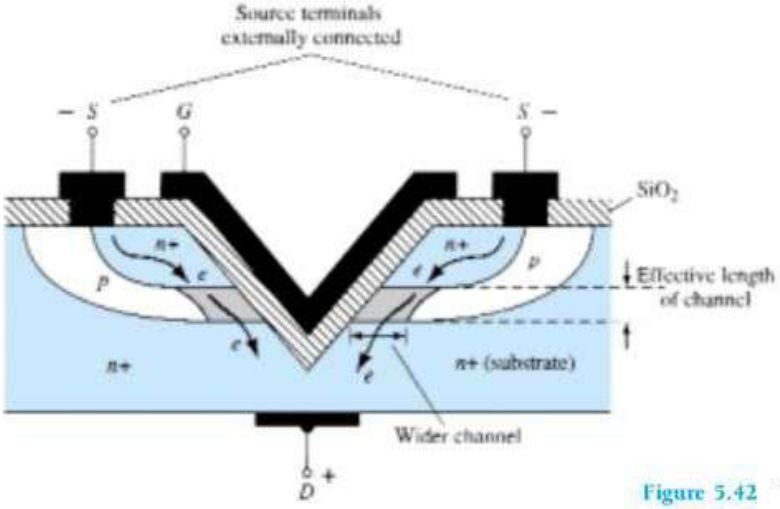

Figure 5.42 VMOS construction.

I_{DSS}/V_P

mode operation). The term *vertical* is due primarily to the fact that the channel is now formed in the vertical direction rather than the horizontal direction for the planar device. However, the channel of Fig. 5.42 also has the appearance of a "V" cut in the semiconductor base, which often stands out as a characteristic for mental memorization of the name of the device. The construction of Fig. 5.42 is somewhat simplistic in nature, leaving out some of the transition levels of doping, but it does permit a description of the most important facets of its operation.

The application of a positive voltage to the drain and a negative voltage to the source with the gate at 0 V or some typical positive "on" level as shown in Fig. 5.42 will result in the induced *n*-channel in the narrow *p*-type region of the device. The length of the channel is now defined by the vertical height of the *p*-region, which can be made significantly less than that of a channel using planar construction. On a horizontal plane the length of the channel is limited to 1 to 2 μm (1 μm = 10^{-6} m). Diffusion layers (such as the *p*-region of Fig. 5.42) can be controlled to small fractions of a micrometer. Since decreasing channel lengths result in reduced resistance levels, the power dissipation level of the device (power lost in the form of heat) at operating current levels will be reduced. In addition, the contact area between the channel and the n^+ region is greatly increased by the vertical mode construction, contributing to a further decrease in the resistance level and an increased area for current between the doping layers. There is also the existence of two conduction paths between drain and source, as shown in Fig. 5.42, to further contribute to a higher current rating. The net result is a device with drain currents that can reach the ampere levels with power levels exceeding 10 W.

In general:

Compared with commercially available planar MOSFETs, VMOS FETs have reduced channel resistance levels and higher current and power ratings.

An additional important characteristic of the vertical construction is:

VMOS FETs have a positive temperature coefficient that will combat the possibility of thermal runaway.

If the temperature of a device should increase due to the surrounding medium or currents of the device, the resistance levels will increase, causing a reduction in drain current rather than an increase as encountered for a conventional device. Negative temperature coefficients result in decreased levels of resistance with increases in temperature that fuel the growing current levels and result in further temperature instability and thermal runaway.

Another positive characteristic of the VMOS configuration is:

The reduced charge storage levels result in faster switching times for VMOS construction compared to those for conventional planar construction.

In fact, VMOS devices typically have switching times less than one-half that encountered for the typical BJT transistor.

5.11 CMOS

A very effective logic circuit can be established by constructing a *p*-channel and an *n*-channel MOSFET on the same substrate as shown in Fig. 5.43. Note the induced *p*-channel on the left and the induced *n*-channel on the right for the *p*- and *n*-channel devices, respectively. The configuration is referred to as a *complementary MOSFET* arrangement (CMOS) that has extensive applications in computer logic design. The relatively high input impedance, fast switching speeds, and lower operating power levels of the CMOS configuration have resulted in a whole new discipline referred to as *CMOS logic design.*

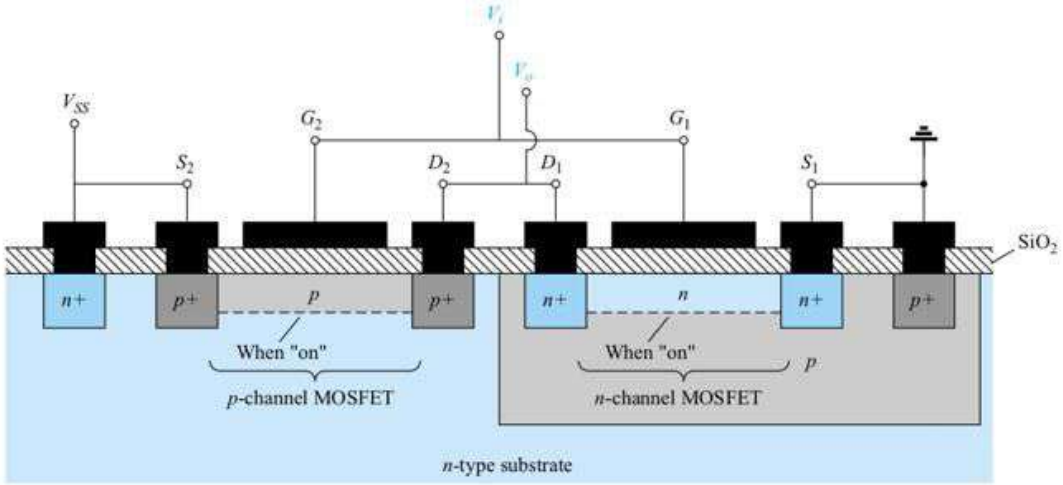

Figure 5.43 CMOS with the connections indicated in Fig. 5.44.

One very effective use of the complementary arrangement is as an inverter, as shown in Fig. 5.44. As introduced for switching transistors, an inverter is a logic element that "inverts" the applied signal. That is, if the logic levels of operation are 0 V (0-state) and 5 V (1-state), an input level of 0 V will result in an output level of 5 V, and vice versa. Note in Fig. 5.44 that both gates are connected to the applied signal and both drain to the output V_o. The source of the p-channel MOSFET (Q_2) is connected directly to the applied voltage V_{SS}, while the source of the n-channel MOSFET (Q_1) is connected to ground. For the logic levels defined above, the application of 5 V at the input should result in approximately 0 V at the output. With 5 V at V_i (with respect to ground), $V_{GS_1} = V_i$ and Q_1 is "on," resulting in a relatively low resistance between drain and source as shown in Fig. 5.45. Since V_i and V_{SS} are at 5 V, $V_{GS_2} = 0$ V, which is less than the required V_T for the device, resulting in an "off" state. The resulting resistance level between drain and source is quite high for Q_2, as shown in Fig. 5.45. A simple application of the voltage-divider rule will reveal that V_o is very close to 0 V or the 0-state, establishing the desired inversion process. For an applied voltage V_i of 0 V (0-state), $V_{GS_1} = 0$ V and Q_1 will be off with $V_{SS_2} = -5$ V, turning on the p-channel MOSFET. The result is that Q_2 will present a small resistance level, Q_1 a high resistance, and $V_o = V_{SS} = 5$ V (the 1-state). Since the drain current that flows for either case is limited by the "off" transistor to the leakage value, the power dissipated by the device in either state is very low. Additional comment on the application of CMOS logic is presented in Chapter 17.

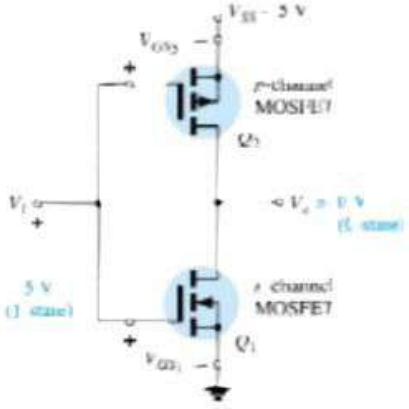

Figure 5.44 CMOS inverter.

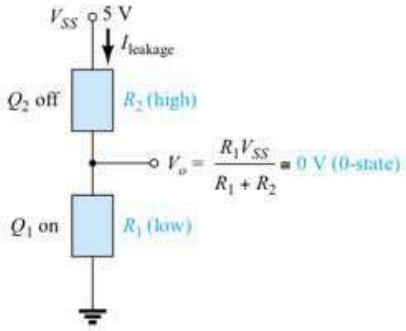

Figure 5.45 Relative resistance levels for $V_i = 5$ V (1-state).